REMARKS

In response to the Office Action mailed December 3, 2003, Applicants respectfully request reconsideration. To further the prosecution of this application, claim amendments and arguments are submitted herewith.

Claims 1, 4, 6-9, 11, 12, 15, 17-20, 22, 23, 26, 28-31 and 33-36 were pending in this application. By this amendment, Applicants have amended claims 1, 12, and 23 for the sole purpose of clarification. Therefore, claims 1, 4, 6-9, 11, 12, 15, 17-20, 22, 23, 26, 28-31 and 33-36 are pending with claims 1, 9, 12, 20, 23 and 31 being independent claims.

Claim Rejections

Claims 1, 9, 12, 20, 23, and 31 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over U.S. Patent No. 5,289,587 to Razban in view of U.S. Patent No. 5,828,824 to Swoboda. Applicants respectfully traverse this rejection.

A. Discussion of Razban

As discussed in the Applicants' previous response, Razban is directed to a method for providing a microprocessor's program counter value external to a device on a dedicated bus so that an external in-circuit emulator system can generate a list of executed instruction addresses (col. 1, lines 17-21). Specifically, Razban provides a virtual program counter value to an external in-circuit emulation system via a dedicated external bus (col. 4, lines 35-41; col. 4, line 66 - col. 5, line 4). Referring to Figure 1, a microprocessor 10 includes a program counter register 28 within execution unit 16 (col. 3, lines 12-15, lines 50-53). Referring to Figure 2, the microprocessor 10 provides the virtual program counter from the program counter register 28 for each instruction that is executed (col. 4, lines 35-38). The virtual program counter is provided via 16-bit external bus 30 (col. 4, lines 38-39). Referring to Figure 3, the virtual program counter is provided in two clock cycles of BCLK, synchronized to active low signal program fetch status (PFS) (col. 4, lines 38-41). The PFS signal is activated whenever a new instruction begins execution, so that the program counter register value is output on bus 30 at that time (col. 4, lines 48-52). Razban states:

> If an exception occurs during execution of an instruction, microprocessor 10 will trap via its conventional trap mechanism. The next virtual program counter value to be sent out on the bus 30 in synchronization to the next PFS signal will be that of the first instruction of the trap routine. (col. 4, lines 53-58)

Razban does not specify the type of exception that may occur, but merely states that when an exception occurs the instructions of a trap routine will then be executed. Thus, the virtual program counter provided on the bus 30 will be that of the instructions of the trap routine. Razban does not discuss transmitting to a debug circuit a status signal.

B. Discussion of Swoboda

Swoboda teaches a method using extended operating modes for debugging an integrated circuit containing multiple modules (Abstract). For example, a system containing a CPU core can be debugged (col. 8, lines 50-54). Figure 1 illustrates a debug environment for connecting high level debugging software to a low level debug interface (col. 8, lines 51-54). The three parts of the debug environment are the debug host 100, the access adapter 102, and the target system 104 (col. 8, lines 54-56). The target system 104 contains one or more CPU cores, which contain hardware to ease the chore of debugging (col. 9, lines 8-10). CPU core debug facilities are provided and allow the user to control program execution in real-time and stop mode debug modes (col. 9, lines 11-15). The stop mode debug facilities can be used to halt program execution after any instruction at any point in the program (col. 7, lines 31-33). Alternatively, the real-time debug facilities insulate time critical portions from debug activity (col. 7, lines 35-37). The time critical portions of the application execute continually while the remaining portions are debugged in a conventional manner (col. 7, lines 37-40). In other words, the time critical portions are not debugged, but rather, are allowed to execute continually so that they are not halted by the debugging operation.

C. Claims 1, 12, and 23 Distinguish Over the Combination of Razban and Swoboda

Claim 1

Claim 1, as amended, recites a microcomputer comprising at least one processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same

integrated circuit, and a system bus coupling the at least one processor and debug circuit. The claim further recites a communication link coupling the at least one processor and debug circuit, wherein the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the at least one processor, and wherein the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the at least one processor. The at least one processor is further configured to transmit to the debug circuit through the communication link a status signal indicating that a computer instruction in the writeback stage is a valid computer instruction, the status signal comprising at least one bit.

Support for the amendments to claim 1 can be found in the written description as filed, for example at: page 4, lines 1-7; page 4, lines 14-15; and page 9, lines 3-6. In a non-limiting example, the claimed status signal reads on PC valid 202 in Figure 2.

The Office Action asserts that the dedicated bus 30 of Razban corresponds to the claimed communication link. Applicants respectfully disagree. As mentioned in section A of this response, the dedicated bus 30 of Razban is used to provide a virtual program counter value of a microprocessor. However, Razban does not teach or suggest at least one processor configured to transmit to the debug circuit **through the communication link a status signal** indicating that a computer instruction in the writeback stage is a valid computer instruction, **the status signal comprising at least one bit**, as claimed. Razban merely indicates that a virtual program counter is provided on the dedicated bus.

Moreover, on page 8 of the Office Action, it is asserted that entering into a trap routine, as taught by Razban, provides a status of the computer instruction, and having an exception occur is an indication that the computer instruction is not valid. Applicants respectfully disagree. An exception may occur in situations other than in response to a computer instruction being invalid, and Razban does not teach that if an exception occurs the computer instruction is invalid. Furthermore, even if entering into a trap routine did "provide" a status of the computer instruction, Razban does not teach or suggest transmitting through a communication link a status signal comprising at least one bit, as claimed.

Swoboda fails to teach the cited limitations of claim 1 that are lacking in Razban. Thus, Applicants contend that claim 1 distinguishes over any combination of Razban and Swoboda.

Additionally, claim 1 requires, *inter alia*, that the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value. The Office Action asserts, on page 2, that the real time limitation corresponds to the real-time debug environment of Swoboda. However, as mentioned in section B of this response, the real-time debug facilities of Swoboda do not provide real time debugging, but rather "insulate time critical (interrupt driven) portions from debug activity" (col. 7, lines 35-37). Thus, debugging is not performed on the time critical portions. Applicants respectfully assert that the combination of Swoboda and Razban in this regard fails to teach or suggest the cited claim limitations.

Thus, claim 1 clearly distinguishes over any combination of Razban and Swoboda, and Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Claims 4, 6-8, and 11 depend from claim 1 and are allowable for at least the same reasons.

Claim 12

Claim 12, as amended, recites a microcomputer comprising at least one processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit, and a system bus coupling the at least one processor and debug circuit. The claim further recites means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the at least one processor, wherein the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the at least one processor. Claim 1 further requires that the at least one processor includes means for transmitting to the debug circuit a status signal indicating that a computer instruction in the writeback stage is a valid computer instruction, the status signal comprising at least one bit. Support for the amendments to claim 12 can be found in the same portions of the application as those discussed above in connection with claim 1.

As discussed in connection with claim 1, above, the combination of Razban and Swoboda fails to teach or suggest multiple limitations of claim 12. Specifically, the combination of Razban and Swoboda fails to teach or suggest means for transmitting to the debug circuit **in real time**, a program counter value. In addition, the combination of Razban and Swoboda fails to teach or suggest at least one processor including means for transmitting to the debug circuit **a status signal** indicating that a computer instruction in the writeback stage is a valid computer instruction, **the status signal comprising at least one bit**. Thus, Applicants respectfully request that the rejection of claim 12 under 35 U.S.C. § 103(a) be withdrawn.

Claims 15, 17-19, 22, and 35 depend from claim 12 and are allowable for at least the same reasons.

Claim 23

Claim 23, as amended, recites a method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit. The method comprises steps of transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor, wherein the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor. The claim further requires that the method comprise a step of transmitting to the debug circuit on the communication link a status signal indicating that a computer instruction in the writeback stage is a valid computer instruction, the status signal comprising at least one bit. Support for the amendments to claim 23 can be found in the same portions of the application as those discussed above in connection with claim 1.

As discussed in connection with claims 1 and 12, above, the combination of Razban and Swoboda fails to teach or suggest all the claimed limitations. Specifically, the combination of Razban and Swoboda does not teach or suggest transmitting, **in real time** to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value. Furthermore, the combination of Razban and Swoboda does not teach a method comprising a step of transmitting to the debug circuit on the communication link **a status signal** indicating that a computer instruction in the writeback stage is a valid computer instruction, **the status**

signal comprising at least one bit. Thus, Applicants respectfully request that the rejection of claim 23 under 35 U.S.C. § 103(a) be withdrawn.

Claims 26, 28-30, 33, and 36 depend from claim 23 and are thus allowable for at least the same reasons.

D. Claims 9, 20, and 31 Distinguish Over the Combination of Razban and Swoboda

Claim 9

Claim 9 is directed to a microcomputer comprising at least one processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit, and a system bus coupling the at least one processor and debug circuit. The microcomputer further comprises a communication link coupling the at least one processor and debug circuit, wherein the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the at least one processor, and wherein the debug circuit is adapted to generate trace information including the program counter.

As mentioned in section C of this response, in connection with claim 1, the combination of Razban and Swoboda fails to teach or suggest a microcomputer comprising, *inter alia*, at least one processor configured to transmit to the debug circuit through the communication link **in real time**, a program counter value. While the Office Action asserts that Swoboda teaches a real-time debug facility, Applicants respectfully contend that the debug facility of Swoboda does not correspond to the claimed real time limitation. The combination of Razban and Swoboda does not teach or suggest the claimed real-time limitation. Accordingly, Applicants respectfully request that the rejection of claim 9 under 35 U.S.C. § 103(a) be withdrawn.

Claim 20

Claim 20 recites a microcomputer comprising at least one processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit, and a system bus coupling the at least one processor and debug circuit. The microcomputer further comprises means for transmitting to the debug circuit in real time, a

program counter value indicating the program counter of the at least one processor, wherein the debug circuit includes means for generating trace information including the program counter.

As discussed in section C of this response, in connection with claim 1, the combination of Razban and Swoboda does not teach or suggest the claimed means for transmitting to the debug circuit **in real time**, a program counter value. Accordingly, Applicants respectfully request that the rejection of claim 20 under 35 U.S.C. § 103(a) be withdrawn.

Claim 31

Claim 31 is directed to a method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit. The method comprises steps of transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor, and further comprising a step whereby the debug circuit generates trace information including the program counter.

As discussed in section C of this response, the combination of Razban and Swoboda does not teach or suggest the claimed method comprising, *inter alia*, transmitting, **in real time** to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value. Accordingly, Applicants respectfully request that the rejection of claim 31 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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